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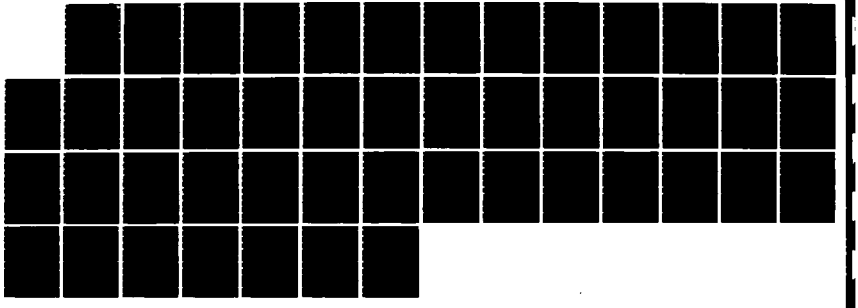

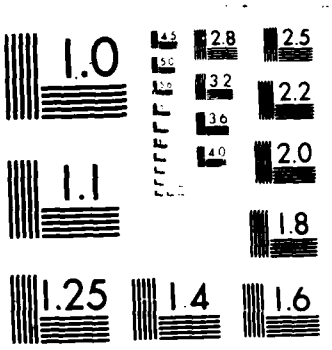

AFGL-TR-86-0242

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Engineering and Instrumentation Support of the AFGL Rocket Research Program

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Final Report:
8 June 1982 - 31 March 1986

7 November 1986

Air Force Geophysics Laboratory
Air Force Systems Command
United States Air Force
Hanscom Air Force Base, Mass. 01731

"This Technical Report has been reviewed and is approved for publication"

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FOR THE COMMANDER

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Division Director

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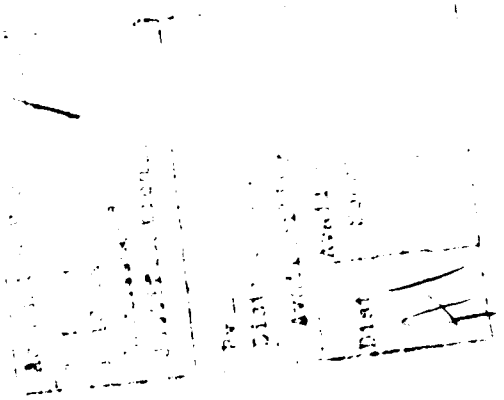

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The Physical Science Laboratory (PSL) of New Mexico State University provided technical support to AFGL over a four year period in the testing, firing, and collection of telemetry data involving sounding rocket payloads. In addition PSL provided software system analysis in support of the CIRRIS project and designed specialized hardware for telemetry ground systems. The hardware included a PCM Bit Synchronizer, PCM Decommutator, and a Portable PCM Ground Station. Software was developed for the system which PSL designed, assembled, and tested.

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1.0 INTRODUCTION

The objective of this contract was to provide engineering and instrumentation support for the Air Force Geophysics Laboratory (AFGL) Rocket Research Program. Specific task areas supported, as authorized by AFGL, included mission support planning, operation and maintenance of GFE equipment, safety systems integration and checkout, development and operation of enhanced PCM Telemetry systems, coordination of technical effort, and developmental studies.

The following PSL engineers contributed to this effort:

Name	Function
A. Gilcrease	FDV, Division Mgr. (Principal Investigator) (6/82 - 6/85)
D. Bawcom	FAB, Branch Mgr. (Principal Investigator) (7/85 - 3/86)
K. Lane	FABS Section Chief (Alternate Principal Investigator)
W. Harkey	Engineer
R. Wagner	Engineer
H. Shaw	Engineer
D. Terwilliger	Engineer
L. Cunningham	Engineer
F. Lawrence	Engineer

2.0 TECHNICAL PROGRESS SUMMARY

The technical progress in this contract centered on the development and fabrication of hardware and software related to PCM decommutators and data collection. Several interfaces between telemetry equipment and peripheral equipment were also designed.

2.1 MANAGEMENT SUMMARY

Management personnel provided financial and schedule tracking with no major problems encountered during the tenure of this contract.

In July 1985, performance of the services of this contract were changed over from Mr. A. Gilcrease to the direct supervision of Mr. D. Bawcom, Principal Investigator, and Mr. K. Lane, Alternate Principal Investigator.

2.2 EQUIPMENT MAINTENANCE

Routine maintenance of station equipment was performed as necessary.

2.3 DAC RESEARCH

The development of a non-volatile, programmable digital to analog converter (DAC) system for the PCM telemetry system, its significance and application were addressed in Scientific Report No. 1, AFGL-TR-83-0199 (ADA137878) entitled "Development of a Non-Volatile Programmable Digital to Analog Converter Subsystem for PCM Telemetry Systems" (PSL PCM DECOM Model 82A) submitted to AFGL in October 1983.

2.4 ROCKET SUPPORT

2.4.1 Rocket A31.200 (SES) (10/82-10/83)

Astrobee "F" Rocket No. A31.200 was successfully launched on 1 March 1983. Launch operation support included rocket preparation, telemetry checks, horizontal and vertical test, operation of telemetry ground stations during launch, data recording during launch and flight and subsequent playback of data.

2.4.2 Rocket A04.902 (UV) (11/82-10/83)

Aerobee 170 Rocket No. A04.902 (UV) was successfully launched on 19 April 1983. Launch operations support included rocket preparation, telemetry checks, horizontal and vertical test, operation of telemetry ground stations during launch, data recording during launch and flight and subsequent playback of data.

2.4.3 Rocket A24.260(ELC-1) (11/82-7/84)

Aries Rocket No. A24.260(ELC-1) was successfully launched on 25 October 1983. Launch operation support included rocket preparation, coordination of telemetry checks, operation of telemetry ground stations (including the AFGL Enhanced PCM Telemetry Station) during all pre-flight tests and the launch, and subsequent playback of data after launch.

2.4.4 Rocket A19.250(Bert) (7/85-3/86)

Sounding Rocket A19.250 was successfully launched on 14 June 1985. Launch operation support included rocket preparation, telemetry checks, horizontal and vertical test, operation of telemetry ground stations during launch, data recording during launch and flight and subsequent playback of data. Data acquisition was nominal except for problems with PCM encoding.

2.5 FIBER OPTICS STUDY

Scientific Report No. 2, AFGL-TR-84-0292 (ADA150852) entitled "Feasibility Study for an AFGL Fiber Optic Data Link at WSMR Sounding Rocket Area" was submitted to AFGL/SULR on 1 October 1984.

2.6 PROGRAMMABLE PCM BIT SYNC

A printed circuit board for the Analog Section of the bit synchronizer was completed. A breadboard of the digital section was also completed. The two sections were integrated and tested from 10 KBPS to 2 MBPS. The unit functioned correctly over this range of data rates for all codes. (Reference Appendix 1)

2.7 DATA DISPLAY SYSTEM

The wire-wrap circuit board for the interface between the data display unit (Astro-Graph 850) and the portable PCM telemetry station was completed in June 1985. Testing of the Astro-Graph 850 Interface revealed several problems in communicating the Astro-Graph device. (Reference Appendix 2)

2.8 LAIRTS STUDY

A report providing information in the development of the LAIRTS Recovery System was submitted to AFGL in July 1983. A plan for developing a breadboard controller system for the LAIRTS was submitted to AFGL in August 1984.

2.9 UPDATE TM STATION

The software support for the AFGL PDP 11/34 Telemetry Station was written during the period 1 June to 16 September 1985 and installed at AFGL during the last week of September 1985. Modifications of the software were made as per AFGL's specifications; AFGL personnel were briefed and demonstrations were given on the use of the software.

Software was written in FORTRAN IV except for the telemetry acquisition driver which was written in MACRO assembly language. The software was run on the RT-11 version 4 operating system. Software was broken up into four inter-related programs, one for each of the four major tasks: program the DECOM, SET UP the data collection parameters, DISPLAY the data and perform POST flight TEST on the data. SET UP used the data generated by DECOM. The data generated by SET UP was later used by both DISPLAY and POST TEST.

2.10 PCM DECOM

A single board UNIBUS PCM Decom/DMA Interface, HS11-A, was fabricated, installed and tested for the AFGL TM station in September 1985. Engineering drawings for the HS-11A cord were submitted to AFGL in October 1986.

The Prototype DAC system was successfully tested on Rockets A31.200 and A24.7S2-3 in March 1983.

2.11 PCM GROUND STATION #1 & #2

The AFGL Enhanced PCM Telemetry Station #1, (MSMP) was completed and equipment shipped to AFGL/LC in November 1982.

The AFGL Enhanced PCM Telemetry Station #2 was completely assembled and checked out. Development of the ELC-1 housekeeping display software was completed in October 1983.

A detailed report entitled "Air Force Geophysics Laboratory Enhanced Portable PCM Telemetry Ground Station" was completed and sent to AFGL/LC in February 1985. See Appendix 3.

2.12 TELEMETRY DATA PROCESSING (RMY)

Software for the AFGL Decom Upgrade was converted from the PDP-11 RSX 11-M Operating System to the VAX-11/750 VMS System. All of the station setup software, digital tape read and write, real-time CRT display, data printing, and data software was converted. The 760 buffer data channel software driver was installed. Cabling for the EMR to Manifold Transition, the Datum to Time Insertion Unit and the cable manifolds were completed. Fabrication of the PAM interface chassis and all software was complete. Phase I System was delivered on 30 April 1984 and Phase II System was delivered in early May.

2.13 CIRRIS SOFTWARE REVIEW

Review of the Video Formatter Programs; was completed and reports were provided to AFGL and USU in December 1983.

A document entitled "Programming Considerations for the NSC 800 Microprocessor in a High Reliability Environment" was prepared by PSL and disseminated to AFGL, Utah State University and Space Data Corporation in December 1983.

A report on the review of the Radiometer Control Electronics Programs was forwarded to AFGL and USU in February 1984.

Review of the Status Controller Program for the Interferometer Control Electronics was completed and report was forwarded to AFGL.

Reports on the SDC Gimbal Control Software review, CIRRIS 1A Interferometer Control Electronics Filter Wheel Control Program; IRIG-B Time Decoder Program, USU's Filter Wheel Controller Program; and the Radiometer Signal Conditioning Electronics were forwarded to AFGL in August 1984.

Review of the sequencer control program was completed and reported in March 1985.

APPENDIX 1
PCM BIT SYNCHRONIZER

The PCM bit synchronizer (bit sync) is to be used on the AFGL PDP11/34A based PCM telemetry system. The desired specifications are:

1. Programmable from PDP11.
2. Frequency range - 10 Kbits/sec to 2 Mbits/sec on all codes.
3. Code types - NRZ-L, NRZ-M, NRZ-S, Biphase-L, Biphase-M, Biphase-S, DM-M, and DM-S.

The PCM bit sync is partitioned as follows: (See Figure 1)

ANALOG SECTION -
* input signal multiplexer
* input signal conditioner
* phase-lock loop

DIGITAL SECTION
* edge detector
* code converter
* output conditioner

Refer to the PCM Bit Sync Schematics, at end of Appendix 1, for the following discussions.

ANALOG SECTION - Input Signal Multiplexer

An external interface connector provides a total of four (4) input PCM serial bit stream signals, IN1 through IN4. Separate return lines are provided for these inputs.

Each PCM input signal is terminated with a 10K-ohm load resistor to ground. A 1K-ohm isolation resistor is placed in series with each PCM input signal.

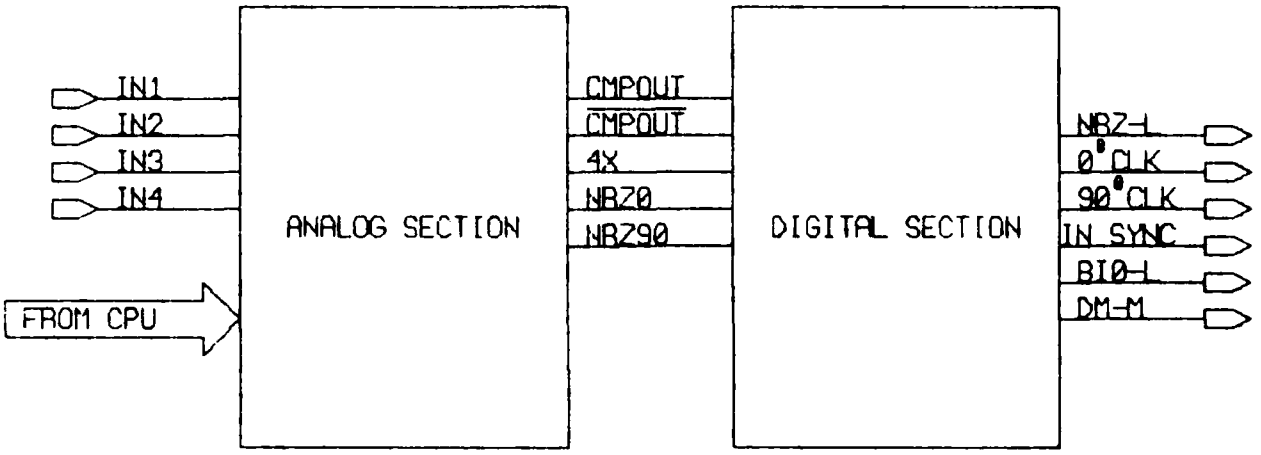


Figure 1

PCM BIT SYNC BLOCK DIAGRAM

The input signal selector (U1) is a Harris HI-524 4-channel video multiplexer. Two bits, SOURCE0 and SOURCE1 from the bit sync control register, control the selection of one of four inputs. The selected output signal appears at pin 2 of U1 and drives the input signal conditioner circuitry.

ANALOG SECTION - Input Signal Conditioner

The input signal conditioner circuitry consists of a high slew rate operational amplifier followed by peak detectors and a high speed differential comparator.

The high slew rate amplifier (U2), Harris HA-2515, has its frequency response controlled by a quad SPST CMOS analog switch (U3), Harris HI-201, which selects combinations of one or more capacitors between its pin 8 and ground. Any combination of four capacitors can be connected at a given time, controlled by signals -INRNG1 through -INRNG4 from the PCM bit sync control register. This provides a programmable low-pass filter function on the selected input.

The peak detectors consist of LM311 comparators (U4, U5) and LM348 amplifiers (U6) connected as followers. The LM311 outputs charge capacitors to establish peak values for each polarity of the conditioned input signal. A HI-201 analog switch (U7) is connected to simultaneously control selection of a peak detector capacitor on the output of each LM311. Two control bit signals, -PDRNG1 and -PDRNG2 from the bit sync control register, control capacitor selection for each peak detector.

DC level signals from the two peak detectors are buffered and added algebraically to establish a midpoint switching threshold for the high speed comparator. The low passed input signal is fed into the high speed comparator (U8), LM361. The switching threshold level is established by the peak detector already described. U8 provides complementary digital output signals, CMPOUT and -CMPOUT, of the analog PCM input signal.

ANALOG SECTION - Phase Lock Loop

A 4X bit rate clock is generated by a Teledyne Philbrick 4743 voltage to frequency (V to F) converter (U11). The 4743 is a 10 MHz V to F and has an input voltage range from 0 to 10 volts.

The raw 4X clock is divided by a two stage D flip-flop counter (U12) into four phased clock signals: NRZ 0 degree, NRZ 90 degree, NRZ 180 degree and NRZ 270 degree. A Hybrid System DAC 9377-16 16 bit digital to analog converter (U9), DAC, supplies the control voltage to the V to F converter. The DAC is loaded by the computer via a 16 bit frequency register. The signal LC loads the DAC.

Signals SUM1 and SUM2, from the digital section, are algebraically added, integrated, amplified and inverted by three LM348 amplifiers (U10). The output from the third LM348 is fed through a Harris HI-201 analog switch (U13) and four loop band width resistors. The output from the resistors is used as the feedback for the phase lock loop circuit, pin 14 (GAIN ADJUST) of the 16 bit DAC. Four control bit signals, -GARNG1 through -GARNG4 from the bit sync control register, control the loop band width of the PCM bit sync.

DIGITAL SECTION - Edge Detector

The edge detector circuit is used to produce a pulse, one-half bit time long, at both the positive and negitive edges of the digital output signals, CMPOUT and -CMPOUT. CMPOUT and -CMPOUT clock both halves of the 74HC74 dual D flip-flop (U14). Both outputs are or'ed/anded (U18,U16) with the 2X clock to produce SUM1 and SUM2. The 74HC161 counter (U15) is enabled at the start of the one-half bit time pulses. U15 counts the 4X clock until pin 13, 1X clock, goes high. This clears both flip-flops (U14) at half bit time and stops the edge detector circuit until the next edge of CMPOUT. SUM1 and SUM2 are used by the phase lock loop to produce the error signal.

DIGITAL SECTION - Code Converter

The code converter circuit converts the incomming digital output signal, CMPOUT, to NRZ-L code and produces a 0 degree clock, biphase-L code (BL) and an in sync signal (IS). The 4X clock is divided by a 74HC161 counter (U17) to produce a 2X clock. POLINV, from the bit sync control register, is used to control the inversion of the incomming digital signal, CMPOUT, at the XOR (U19).

The actual code conversion is done by a "state machine" consisting of a 74HC164 shift register (U20), a 27C64 EPROM (U21) and a 74HC374 octal latch (U22). The output of the XOR, OUT, is fed to the input of U20. The 2X clock is used to clock U20 and latch U22. The selection of the converted code is controlled by C0 and C1. C0 and C1, along with C2 and C3, are derived from PCMCODE0, PCMCODE1, PCMCODE2 and PCMCODE3 from the bit sync control register. The control code table is shown on the schematic.

DIGITAL SECTION - Output Conditioner

The output conditioner circuit is used to generate and buffer the output signals from the bit sync. The six outputs are:

1. NRZ-L code
2. 0 degree clock
3. 90 degree clock
4. IN SYNC
5. Biphase-L code
6. DM-M code

The first four outputs are required by the decom. The last two, biphase-L and DM-M, are optional and are intended for analog tape recordings.

The lower portion of the output conditioner circuit is used only for NRZ-L input code. The input NRZ-L code is used directly and does not go through the "state machine". A 74HC244 octal buffer (U26) is used to buffer the NRZ-L code (OUTN), 0 degree clock, NRZ90 degree and IS. U26 is selected

when C3 is high. The input NRZ-L code is converted to biphase-L and DM-M by U19, U16 and U24. U26 also buffers these two codes.

The upper portion of the output conditioner circuit is used for the remaining input codes. The two XOR's (U19) control the inversion of NL (NRZ-L) and BL (biphase-L) from the "state machine". C2 high will invert NL and BL. This condition will occur when a "S" code is selected. A 74HC244 octal buffer (U25) buffers NL and BL along with 0 degree clock, NRZ90 degree, IS and the converted DM-M code. Biphase-L is inverted by U16 and converted to DM-M by a 74HC74 flip-flop (U23).

STATUS:

The analog section of the bit sync was fabricated on a printed circuit board. A breadboard of the digital section was built using an A.P. Products Inc. ACE (All Circuit Evaluator) 236. The bit sync was tested using a PCM simulator and functioned from 20 Kbits/sec to 2 Mbits/sec. The bit sync should function to 2.5 Mbits/sec. The 2.5 Mbit/sec limit was not tested because the PCM simulator used has a upper limit of 2 Mbits/sec.

The bit sync functioned best at the higher bit rates. At 1 Mbits/sec the loop bandwidth was +-1% with a setablility of +-1% or better. The loop bandwidth and frequency settings at the lower bit rates (less than 50 Kbits/sec) was not acceptable. The PCM code converter was tested with all input codes and functioned properly.

FUTURE WORK:

The feedback circuit on the phase lock part of the VCO needs to be redesigned. This should help the low bit rate problem. A new V to F, DYMEC 3832, is available and should be tested. This may also help the low bit rates. The bit sync needs to be tested with "real" PCM data from one of the AFGL Aries missions. The code converter needs to include the proposed new IRIG PCM codes, differential biphase-M (DBIO-M) and differential biphase-S (DBIO-S). The bit sync needs to be mounted on the HS11-A board in the PDP11/34A or mounted on a separate UNIBUS board.

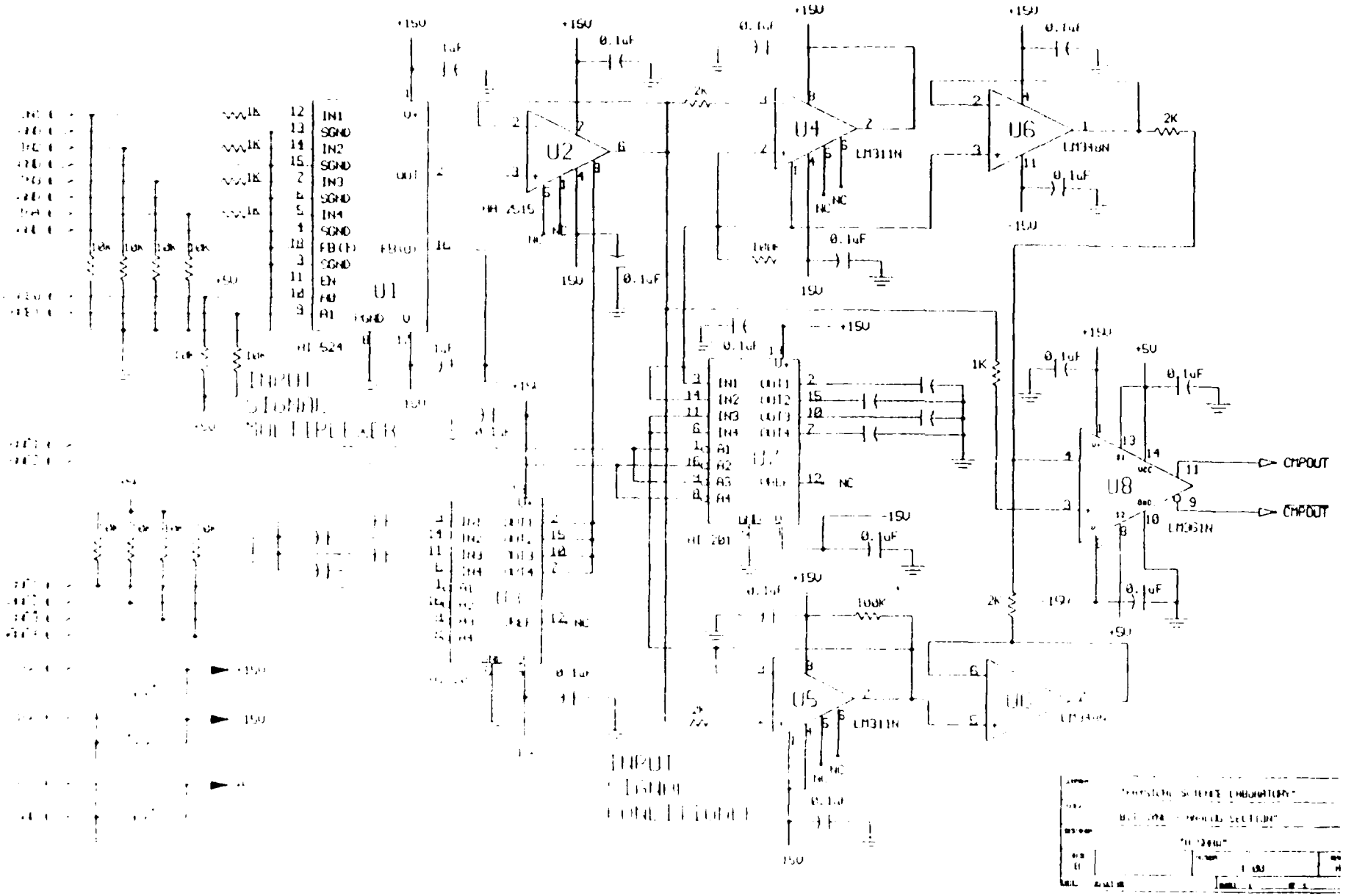


Figure 2 - Unit Cell - Analog Section

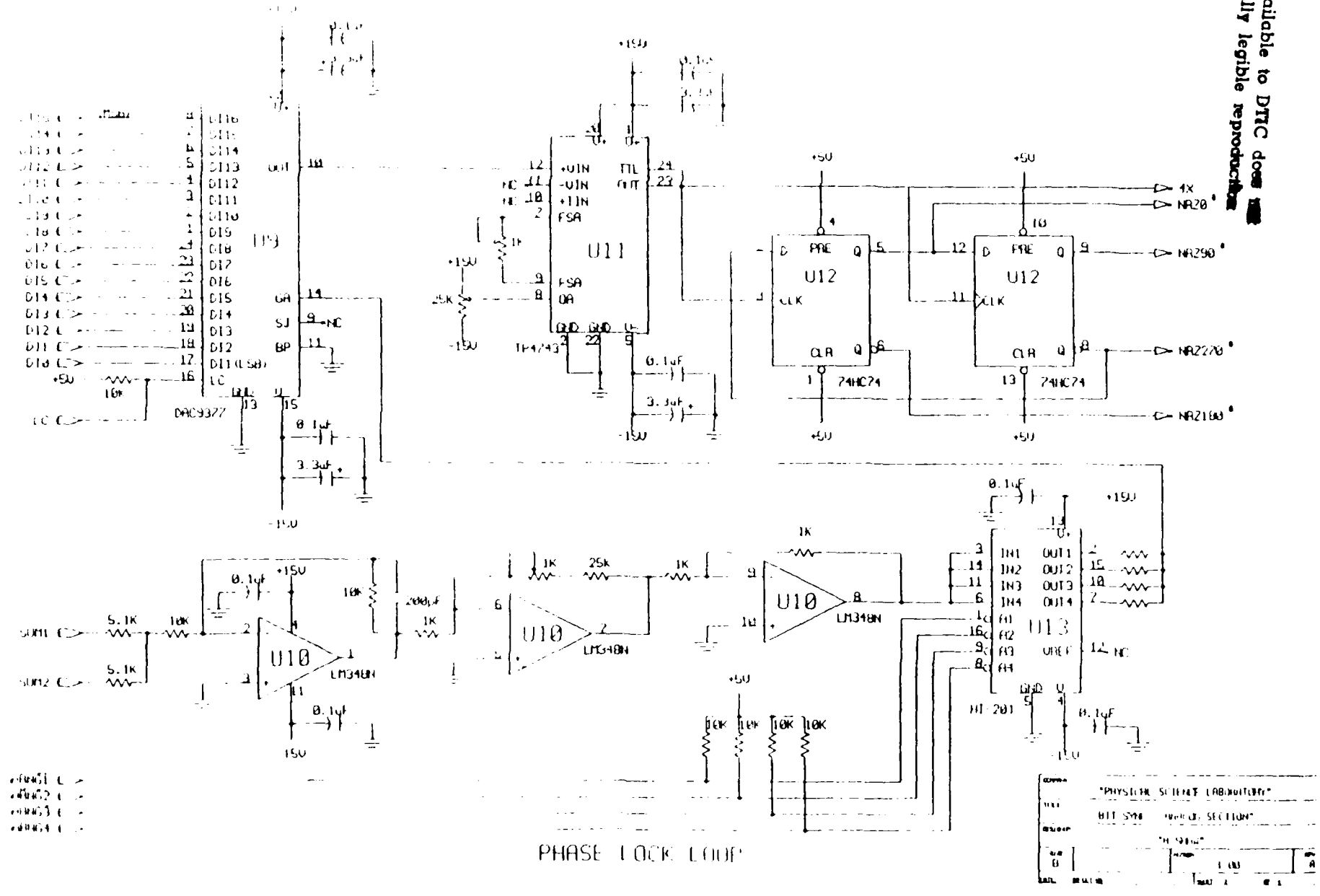


Figure 3 - Bit Sync - Analog Section

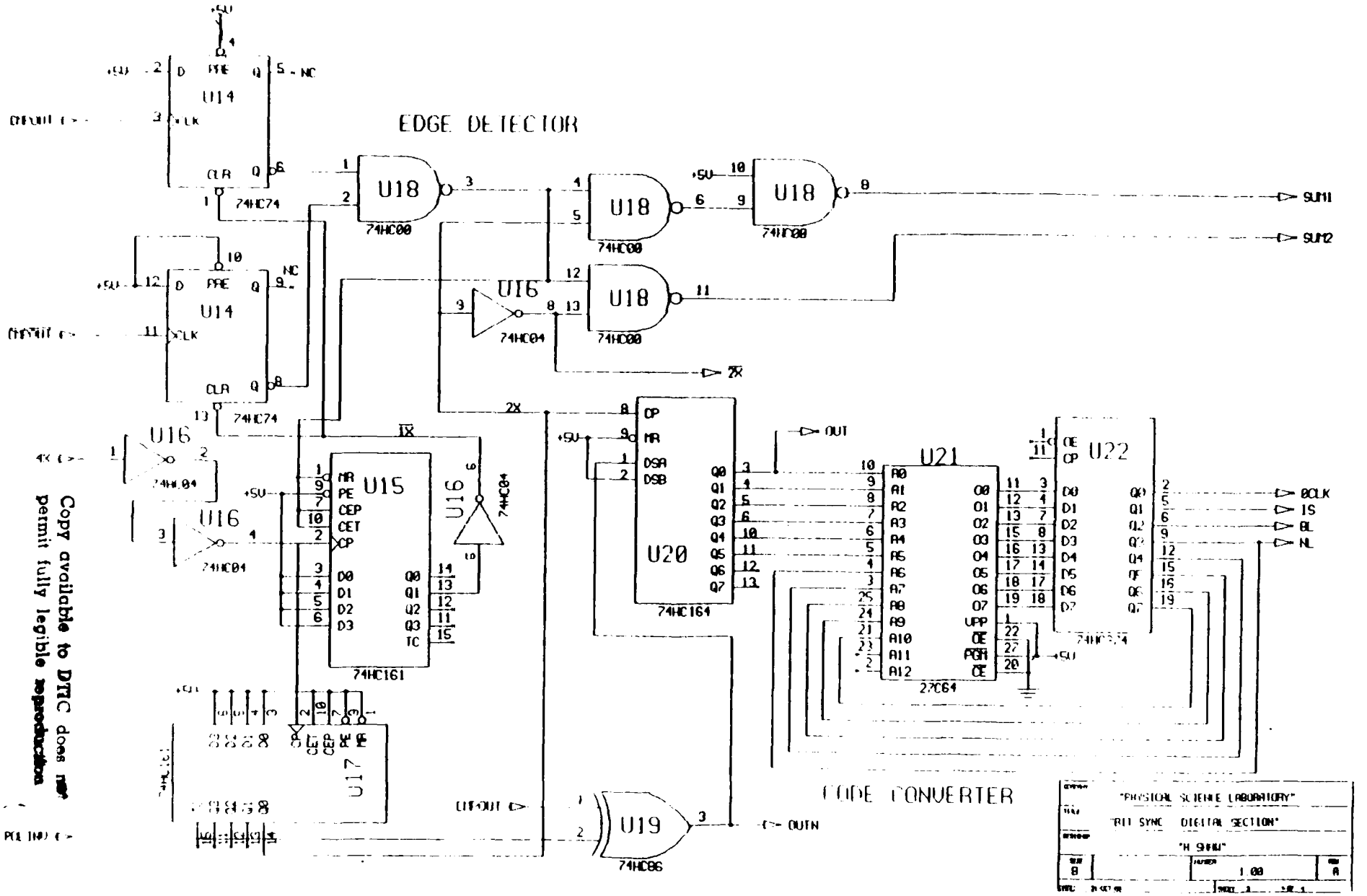
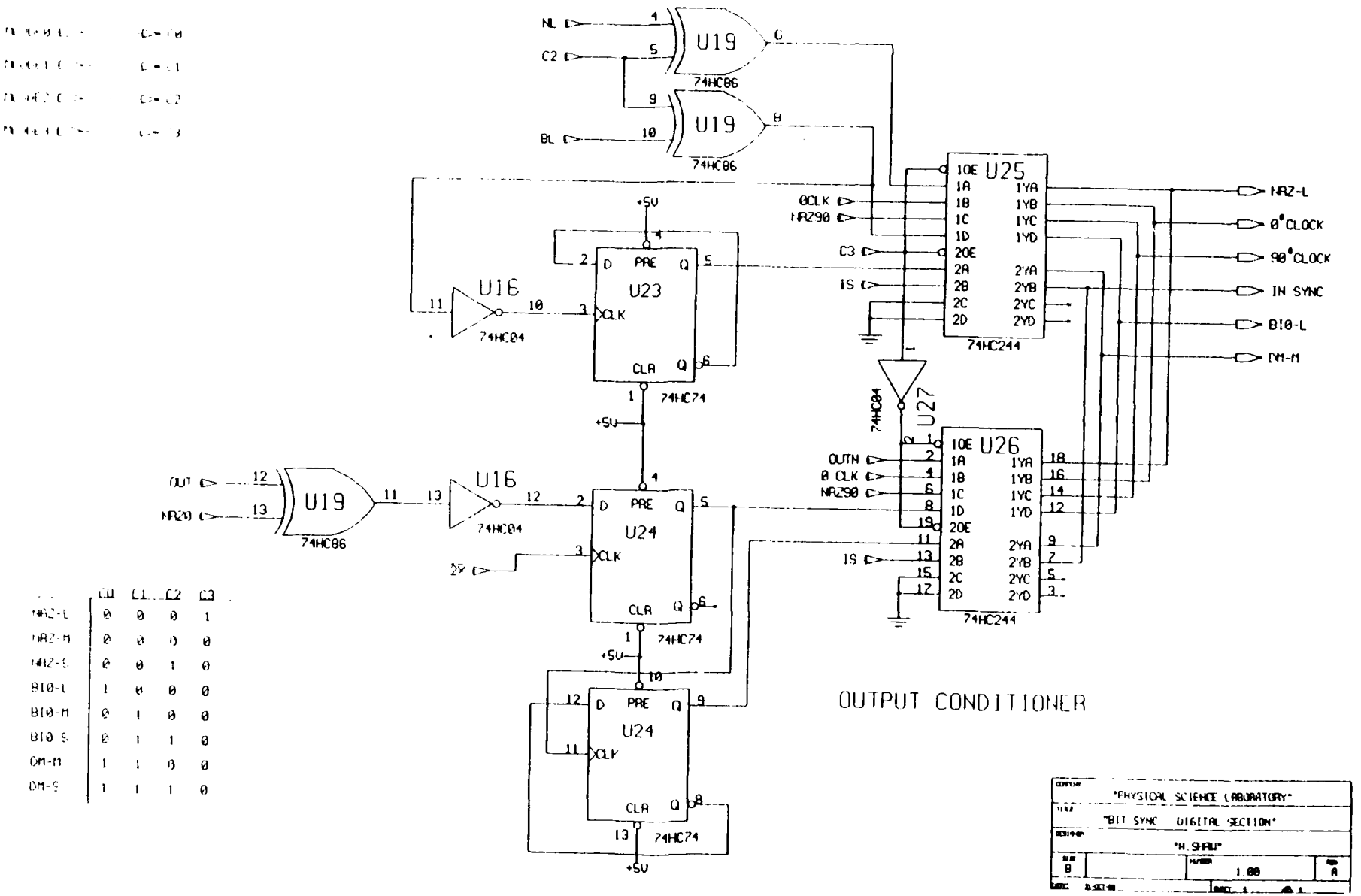


Figure 4 - Bit Sync - Digital Section



	C0	C1	C2	C3
NRZ-L	0	0	0	1
NRZ-M	0	0	0	0
NRZ-S	0	0	1	0
BI0-L	1	0	0	0
BI0-M	0	1	0	0
BI0 S	0	1	1	0
DM-M	1	1	0	0
DM-S	1	1	1	0

Figure 5 - Bit Sync - Digital Section

APPENDIX 2
DATA DISPLAY SYSTEM

The data display system is based on an Astro-Graph Model 850 direct writing digital recorder manufactured by Astro-Med, Inc. The display system interfaces to the AFGL PDP11/34A based PCM telemetry system. The 850 gives the telemetry system strip chart capability. The 850 can present data in the following modes:

1. Bitmap or user control over individual thermal elements of the print head.
2. Line Printer - 80 characters per line, 66 lines per page.
3. Three (3) channels with 12 lines of text.
4. 30 Channels.
5. Block printing and graphics.

Other modes, such as 6 channel, 8 channel, etc., can be selected by a ROM change in the 850 recorder.

Status:

An interface was built on a MDB-1710 general purpose parallel bus foundation module. The MDB-1710 has built in bus interface circuitry and a wire wrap area in which the 850 interface was built. The schematics for the interface are shown in Figures 6, 7, and 8. Preliminary testing of the system was initiated. The interface communicated with the 850 with minimal success. The 850 appears to operate differently than stated in the manual.

Future work:

The operation of the 850 needs to be cleared up. The hardware needs to be modified, if necessary. Once the hardware is working, application software needs to be developed.

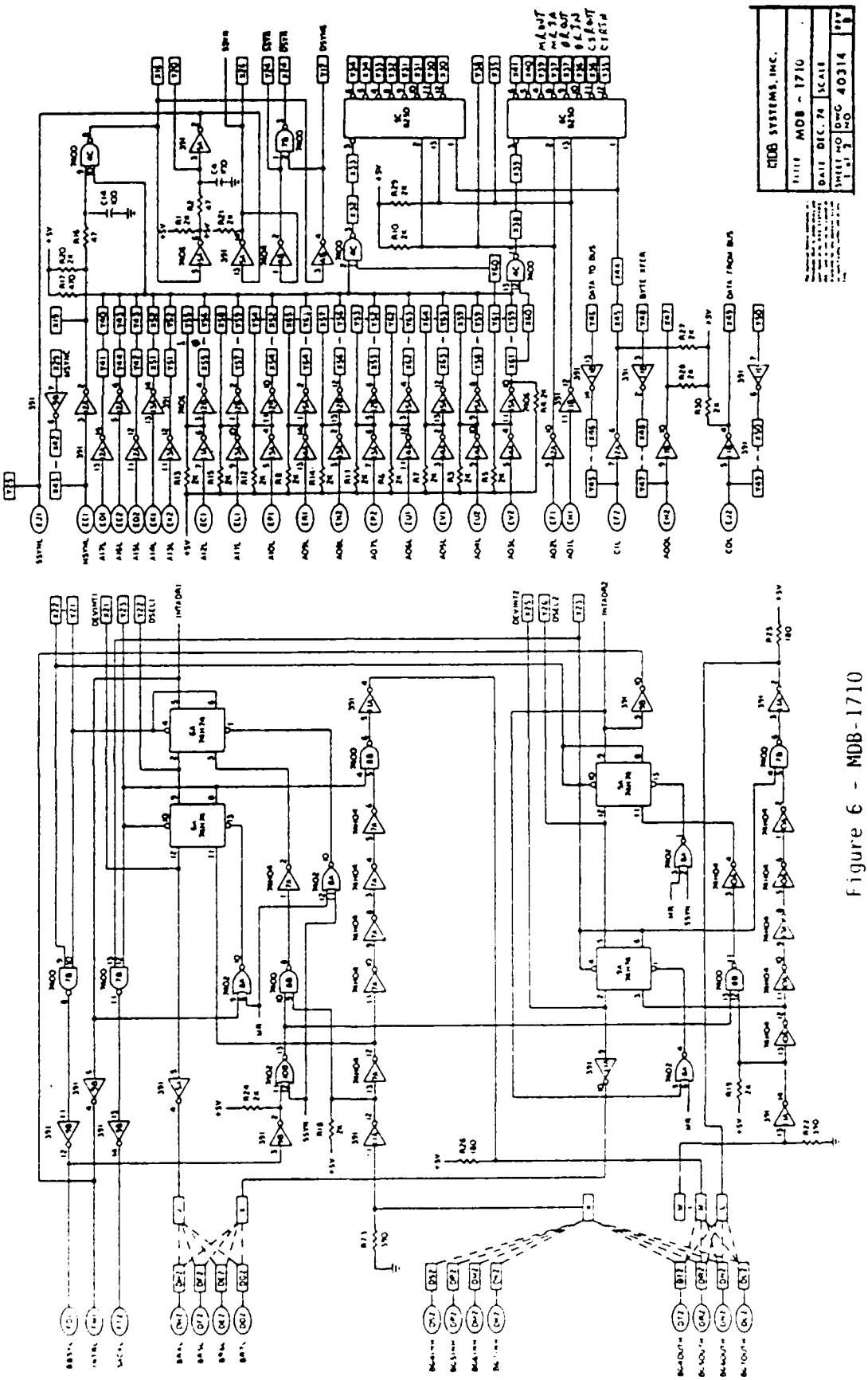


Figure 6 - MDB-1710

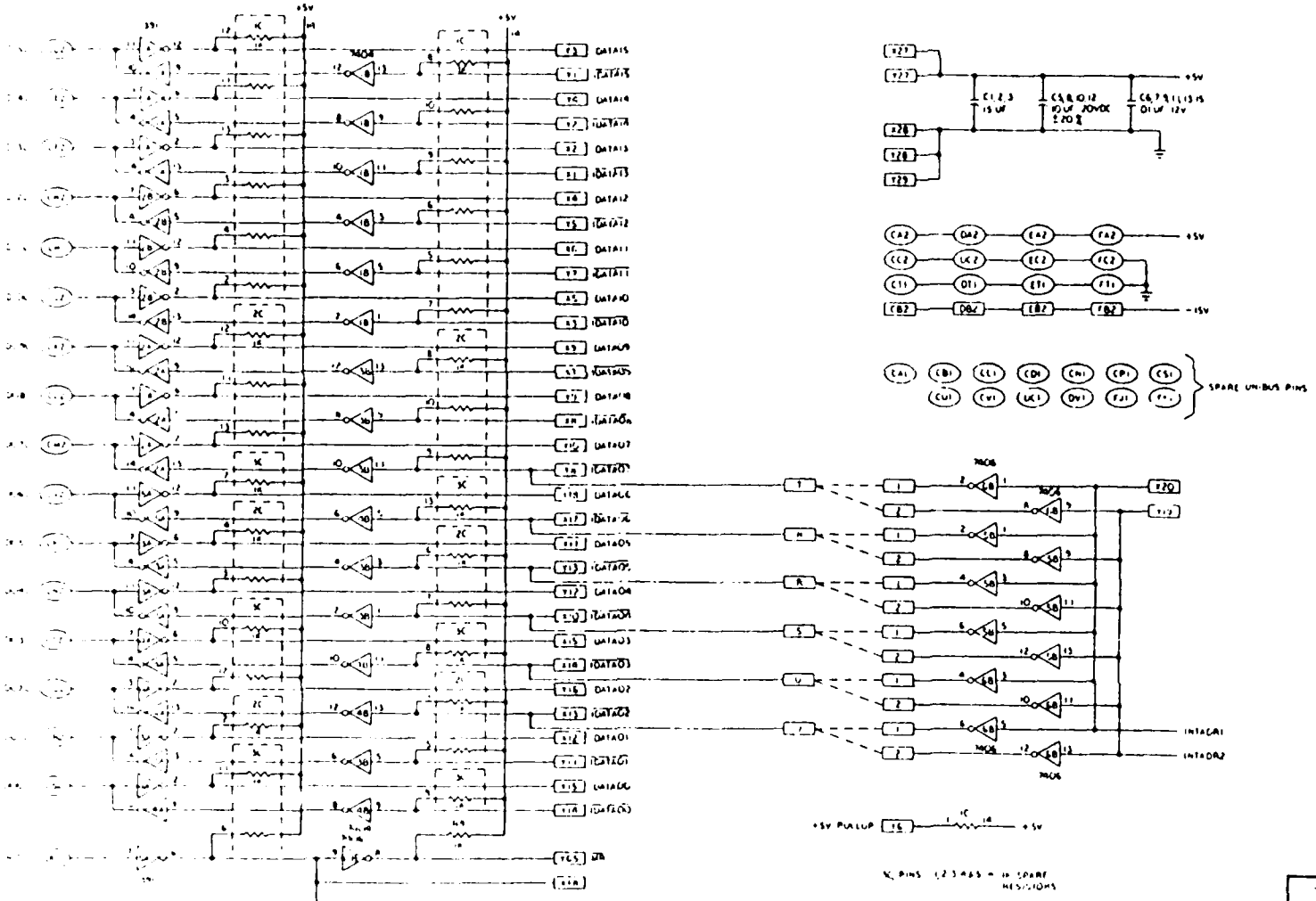


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Figure 7 - MDB-1710

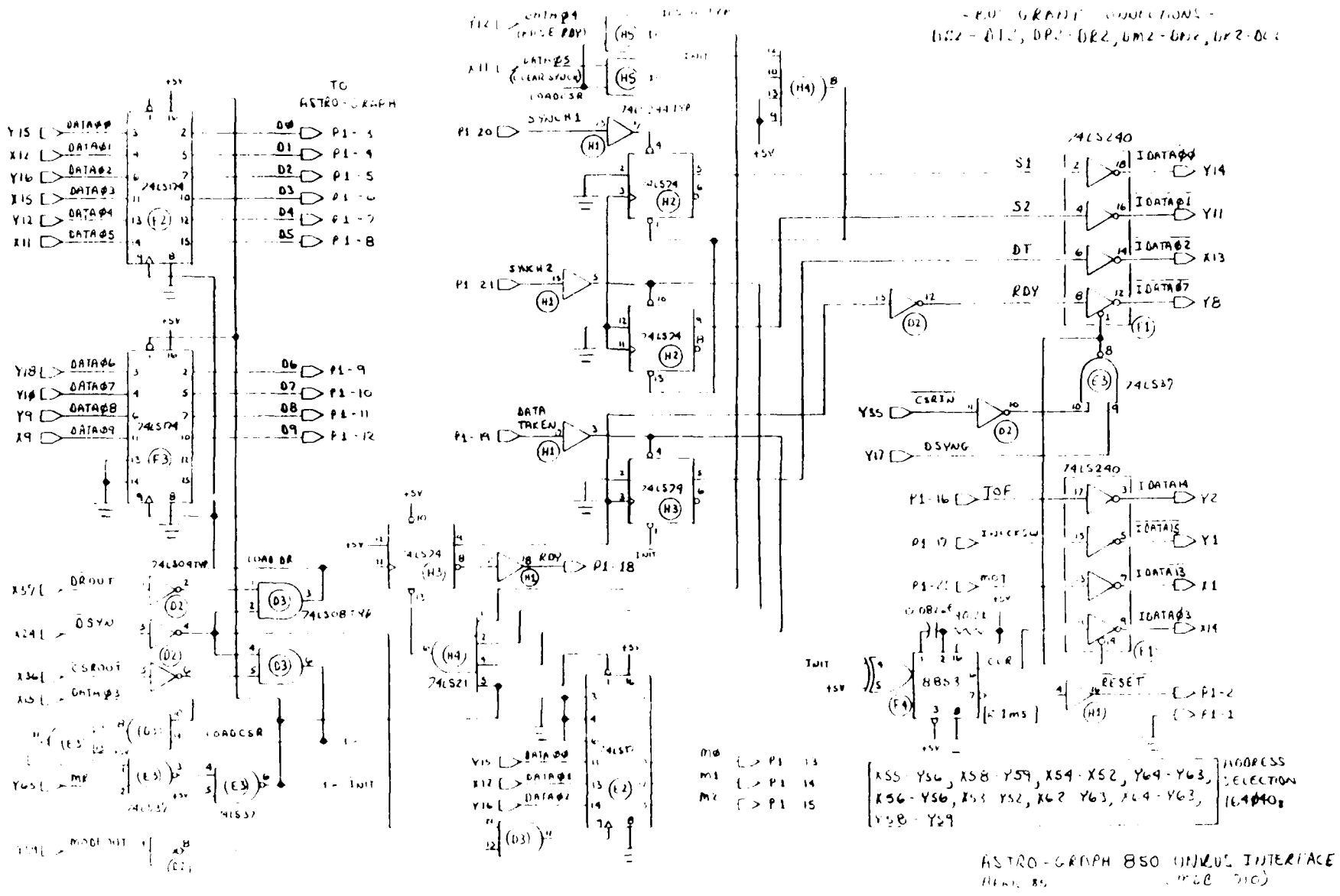


Figure 8 - ASTRO-Graph 850 UNIBUS Interface

APPENDIX 3

AIR FORCE GEOPHYSICS LABORATORY ENHANCED PORTABLE PCM TELEMETRY GROUND STATION

INTRODUCTION

Although sounding rockets and data gathering for sounding rocket payloads have been with us since the late 1940's, a quantum leap in data volume, complexity, and transmission rates took place in the early 1970's with the advent of Pulse-Code Modulation (PCM).

During the 1970's the primary source of digital real-time sounding rocket payload support consisted of large scale digital computer systems located at a few established test ranges. If the researcher required data during the construction and initial testing of the payload or if the rocket were to be fired from a remote site, the researcher had to rely on oscillographs and/or an analog tape which could be reduced at a later date. This situation created a void that could only be filled with a low cost, transportable computer/telemetry interface system utilizing a flexible, high level software system.

BACKGROUND

The Physical Science Laboratory (PSL) has been associated with the Air Force Geophysics Laboratory (AFGL) since the late 1950's. PSL has supplied not only launch support at White Sands Missile Range (WSMR) and other locations, but has designed and built telemetry equipment for various AFGL payloads.

Prior to the advent of PCM telemetry and even during the early days of PCM, the volume and complexity of telemetry data required very little in the way of display capability. A few strip chart traces provided all the information necessary to determine the operational integrity of the payload. However, the complexity of the newer payloads has become such that a computer is needed to determine the integrity of the experiments.

In early 1981, PSL was tasked by AFGL to develop a portable PCM telemetry station that would acquire and support the higher PCM data rates from Aries-type rocket payloads. The station would have to provide real-time and near real-time calibration, prelaunch and launch test support to AFGL researchers involved in space vehicle probe analysis. The station would also have to utilize a flexible software system, transportable hardware, and be easily expanded to meet the continually growing and varied needs of the researchers.

The same portable PCM telemetry station would (could) stay with the experiment/payload from buildup through launch and post flight analysis. This is a good validation of the experiment/payload since the same hardware and software would be used throughout the life of the experiment/payload. Cost savings would be realized in several ways:

1. Availability of immediate test results during payload buildup.
2. No need for large scale computer systems support during payload buildup; i.e., don't have to carry an analog tape elsewhere for digitizing and reduction.
3. Minimal test range support required until launch.
4. No test range computer support required for post-test analysis.

A survey was done by PSL to determine if any hardware existed that would meet the needs of AFGL. Hardware was found that would meet the needs, however, it was not portable. Likewise, the portable hardware found would not meet the required software and expansion needs.

PSL designed, built and operates a PDP-11 computer based PCM telemetry station for NASA at WSMR. This system had a PSL built decom that was external to the computer and was connected to the computer via a PSL built DMA (direct memory access) interface. This system met the AFGL needs and with some redesign could be made portable. The decom was redesigned and combined with the DMA interface on one board that fits on the PDP-11 computer bus (UNIBUS). This redesign saved both weight and rack space. The new DECOM/DMA interface is the heart of the portable PCM telemetry station designed and built for AFGL.

SYSTEM DESCRIPTION

A. Block diagram

The block diagram of the PCM system is shown in Figure 9. The system consists of the following equipment:

1. Computer - Digital Equipment Corp. (DEC) model PDP-11/34A with the following options:
   A. 256 Kbytes of memory
   B. FP11-A floating point processer
   C. KK11-A cache memory
2. Disk system - A DEC RL211 controller with two (2) each DEC model RL02 disk drives (10.4 Mbytes removable disk cartridge each).
3. Console terminal - DEC model VT125 CRT terminal. The VT125 is a graphics terminal with DEC ReGIS protocol.
4. Auxiliary terminals - Two (2) DEC model VT100 CRT terminals. These provide additional non-graphic displays for the system.
5. Asynchronous interface - DEC DZ11 8-line asynchronous multiplexer. The DZ11 provides a RS-232 interface for the auxiliary terminals and the modem.
6. Digital Tape System - Two (2) each Kennedy model 9300 tape drives and Emulex model TC11 tape controller. Each tape drive is 800/1600 BPI at 125 IPS.
7. Line printer - Printronix P300 and interface. The P300 is a dot matrix printer/plotter. Capability is 300 lines per minute in the print mode and 16.7 inches per minute in the plot mode.
8. Time Code Reader/Translator - Datum model 9310.
9. Bit Sync - DSC model 4781.
10. Parallel Interface - MDB model DR11-C. Programs the bit sync.
11. DECOM/DMA Interface - PSL model HS11-A.
12. PCM Simulator - PSL model 82.
13. Modem - Hayes Smartmodem 1200. 300/1200 baud modem.

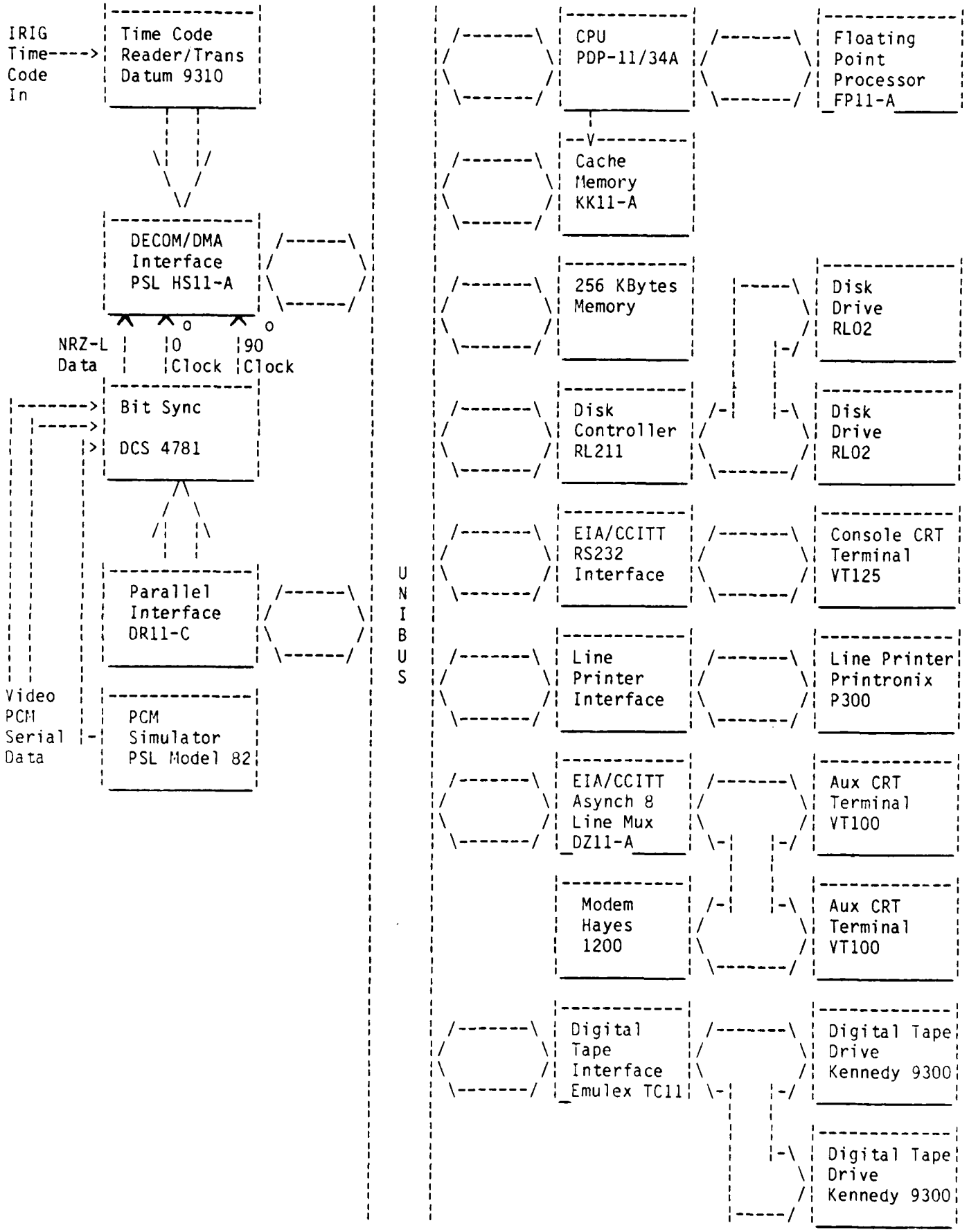


FIGURE 9 - SYSTEM BLOCK DIAGRAM

B. PCM DECOM/DMA Interface (PSL Model HS11-A)

General:

The HS11-A PCM DECOM/DMA interface was developed by PSL for use on a Digital Equipment Corporation (DEC) PDP11 computer. The interface is built on a hex height, extended length, double width wire wrap module board. The interface fits in a small peripheral slot (SPC) in the PDP11 UNIBUS. All power is supplied by the computer system. The interface consists of two (2) sections: a decommutator (DECOM) section and a direct memory access (DMA) section (Figure 10).

The UNIBUS communicates with the HS11-A interface via sixteen (16) device registers. Eight (8) device registers are used in the DECOM section and are shown in Figure 11. The other eight (8) device registers are used in the DMA section, these will be discussed later.

DECOM Section:

The decommutator (DECOM) section of the interface converts the incoming serial PCM data to parallel data for use by the DMA section. The DECOM section takes the NRZ-L serial data and the 0 degree and 90 degree clocks from the bit synchronizer and converts them to 16 bit parallel data and various synchronous timing pulses. For purposes of this discussion, a frame is defined as a minor frame and a subframe as a major frame.

The DECOM section specifications follow:

1. Up to 2.0 megabits/sec.
2. Up to 16 bits/word.
3. Up to 1024 words/frame.
4. Up to 256 frames/subframe.
5. Up to a 64 bit frame sync word.

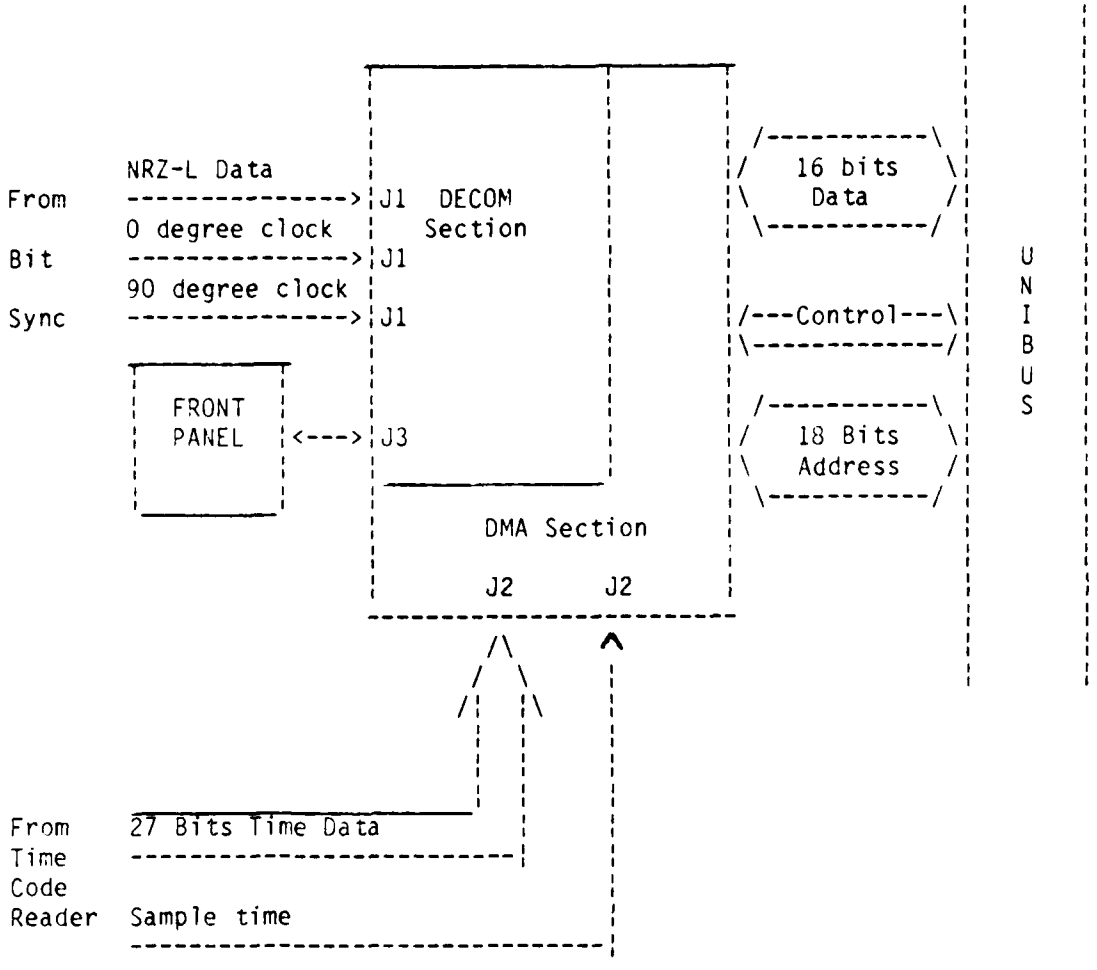
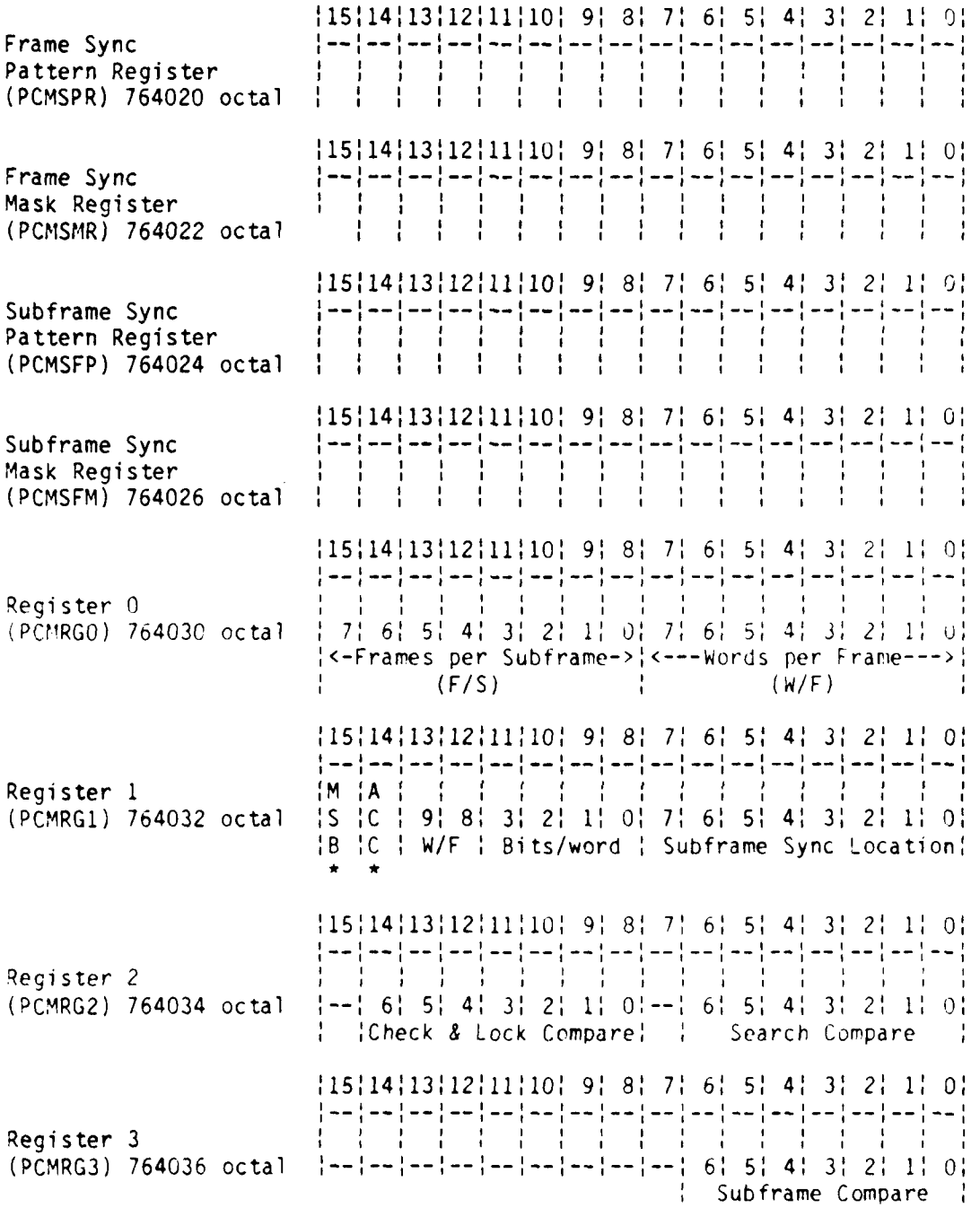


FIGURE 10 - PCM DECOM/DMA INTERFACE BLOCK DIAGRAM



Note:

* MSB=0 => LSB first
MSB=1 => MSB first
ACC=0 => Normal
ACC=1 => Alternate Code Complement

FIGURE 11 - DEVICE REGISTERS/DECOM SECTION

6. Up to a 64 bit subframe sync word, located anywhere in first 256 words of the frame.
7. Most significant bit (MSB) or least significant bit (LSB) first.
8. Normal frame sync or alternate code complement (ACC).

The synchronization (sync) of the PCM data in the interface is handled by two (2) TRW TDC1023J 64 bit monolithic digital correlators: one for the frame sync and the other for the subframe sync. Each digital correlator has three (3) serial 64 bit registers. The REFERENCE register is used to store the sync pattern. The PCM data are shifted through the DATA register and its parallel output is compared (exclusive ORed) with the parallel output of the reference register. The MASK register masks or selectively chooses "no compare" bit positions enabling total length flexibility. The compared and masked parallel data go to a 64 bit pipelined digital summer. The summer outputs are used in the sync circuit for the detection of sync.

There are three (3) states of sync: Search, Check and Lock. These states pertain to both the frame and subframe syncs. The search state is when no correct sync patterns are being detected. One detected correct sync pattern will cause the DECOM to go into the check state. The DECOM will remain in the check state until seven (7) more correct consecutive sync patterns are detected in the correct word(s) and only then will the DECOM go into the lock state. Conversely, the DECOM will remain in the lock state until an incorrect sync pattern is detected. The DECOM will then go into the check state. Seven (7) incorrect consecutive sync patterns will cause the DECOM to go into the search state. The subframe sync will be forced into the search state whenever the frame sync goes into the search state.

The sync pattern detection circuits can handle various bit compares in the sync patterns. The number of bit compares can be set from zero (no bit compare) to the number of sync bits, a maximum of 64 bits. Three (3) registers are used to set the number of sync compares required: Check and Lock Compare, Search Compare and Subframe Compare. The Check and Lock Compare Register holds the number of compare bits in the frame

sync pattern while in the check and lock modes. The Search Compare Register holds the number of compare bits in the frame sync pattern while in the search mode. The Subframe Compare Register holds the number of compare bits in the subframe sync pattern for all three modes: search, check and lock. The usual error scheme for frame sync is N-1 compares (one error) for the search compare and N compares (no errors) for the check and lock compare. The usual error scheme for the subframe sync is N compares (no errors). The Check and Lock Compare Register and the Search Compare Register are located in Register 2 (PCMRG2) and the Subframe Compare Register is located in Register 3 (PCMRG3). The Device Registers for the DECOM section are shown in Figure 11. The HS11-A interface transfers data in two modes. One mode will transfer data only when the data are valid; i.e., interface is in lock state or check state. The other mode will transfer data in any state: search, check or lock. Bit 8, Search Data Xfer, of the Command Status Register (PCMCSR) is used to control these two transfer modes. (Information on the PCMCSR is provided in a following discussion of the DMA Section).

The Frame Sync Pattern Register (PCMSPR) is used to load the frame sync pattern into the interface. This register (16 bits) is parallel loaded by the computer and then serial shifted out to the digital correlator in the sync circuit. This parallel loading in/serial shifting out process must be done four (4) times to load the entire 64 bits in the digital correlator. A logical "1" in the PCMSPR equals a logical "1" in the sync pattern.

The Frame Sync Mask Register (PCMSMR) is used to load the frame mask pattern into the interface. This register is loaded exactly the same as the PCMSPR. This mask register allows the selection of bit positions where no comparisons are desired in the PCMSPR. A logical "0" equals a "no comparison" in the mask register.

The Subframe Sync Pattern (PCMSFP) and Subframe Mask (PCMSFM) Registers are the same as PCMSPR and PCMSMR, respectively, except that they pertain to the subframe.

Register 0 (PCMRG0) is used to hold the words per frame count, 8 bits, and the frames per subframe count, 8 bits. Two more words per frame bits are in the Register 1 (PCMRG1). This brings the total number of words per frame to 1024 (10 binary bits).

Register 1 (PCMRG1) is used to hold subframe sync location, 8 bits, bits per word count, 4 bits, the other two (2) words per frame bits, and the ACC and MSB bits.

Register 2 (PCMRG2) is used to hold the check and lock compare bits for the frame sync, 7 bits. Register 2 is also used to hold the search compare bits for the frame sync, 7 bits.

Register 3 (PCMRG3) is used to hold the subframe compare bits, 7 bits. The nine (9) most significant bits are not used.

DMA Section:

The direct memory access (DMA) section takes the parallel data from the DECOM section and makes it available to the computer. The DMA section replaces the last frame sync word with two (2) timing words, 16 bits each, from a time code reader/translator. This is the only modification the DMA section does to the incoming data. Figure 12 shows the structure of the two (2) timing words and a representation of typical data words.

The data are controlled by three (3) registers: Buffer Address Registers 0 and 1 (PCMBA0 and PCMBA1), and a Word Count Register (PCMWC). The Buffer Address Registers control where in the computer memory the data will be transferred. The DMA interface uses two (2) Buffer Address Registers to transfer the data. These buffers will cycle automatically; i.e., one buffer will be "filling" up with data and the other buffer will be available for reading by a software application program. The Word Count Register is used to control the number of words that are to be transferred to the computer, usually a

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIMING WORD 0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	2 sec	2 sec	2 sec	2 sec	2 sec	2 sec	2 sec	2 sec	2 sec	2 sec	2 sec	2 sec	2 sec	2 sec	2 sec	2 sec

Timing word 0 contains fifteen (15) bits of straight binary time of day in seconds.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIMING WORD 1	16				not	not	9	8	7	6	5	4	3	2	1	0
	2 sec	0	0	0	FL	SL	2 ms	2 ms	2 ms	2 ms	2 ms	2 ms	2 ms	2 ms	2 ms	2 ms

Timing word 1 contains the 17th bit of time of day in seconds, frame not locked, subframe not locked and ten (10) bits of straight binary time in milliseconds. Bits 12, 13 and 14 are set to zero.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA WORDS 1 and 2	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
	<---------DATA WORD 1--------->								<---------DATA WORD 2--------->							

This is a typical data word structure presented to the UNIBUS for 8 bits per word PCM telemetry data. One (1) telemetry word is one (1) byte to the UNIBUS. DATA WORD 1 is defined as the first data word after the last sync word. DATA WORD 1, in this case, would be the most significant 8 bit byte after TIMING WORD 1.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA WORD 1	0	0	0	0	0	0	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
							<----------DATA WORD 1---------->									

This is a typical data word structure presented to the UNIBUS for 10 bits per word PCM telemetry data. One (1) telemetry word is ten (10) bits to the UNIBUS. DATA WORD 1 is defined as the first data word after the last sync word. DATA WORD 1, in this case, would be the first data word after TIMING WORD 1. The six (6) most significant bits are set to zero.

FIGURE 12 - TIMING AND DATA WORD STRUCTURE

multiple of the subframe if present. If not, it will be a multiple of the frame. The time data from the time code reader/translator can also be read into the computer by two (2) registers: Time Data Registers 0 and 1 (PCMTD0 and PCMTD1). The Command Status Register (PCMCSR), shown in Figure 13, is used to control the DMA section. The other seven (7) device registers are shown in Figure 14.

Three (3) I/O (input/output) connectors are used in the HS11-A. Connector J1 is the input from the bit sync. This input contains the NRZ-L data and the 0 and 90 degree clocks needed for the DECOM section. Connector J2 is the input from the time code reader/translator. This input contains the timing information needed for the interface. Connector J3 connects to the front panel of the computer. The front panel of the computer has been modified to contain the circuitry for displaying various functions of the DECOM section; search, check, lock, etc. The displays are for monitoring and trouble shooting the DECOM section.

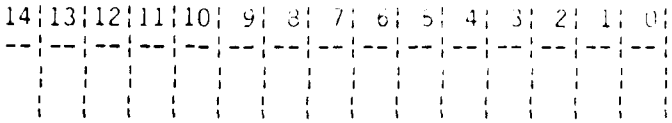
Command Status Register (PCMCSR) 764000 octal

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

BIT	NAME	FUNCTION
15	Error	Set to indicate an error condition: Non-existant memory (NEX, bit 14) or bus address overflow (PCMBA0 or PCMBA1 incremented from all 1's to all 0's). Sets ready (bit 7) and causes Interrupt 0 if Interrupt Enable (bit 6) is set. Error is cleared by Init, setting Clear Interface (bit 3) to a logic '1', or loading PCMBA0. READ ONLY.
14	Non-existent memory (NEX)	Set to indicate that as UNIBUS master, the DMA section did not receive a SSYN response 20 microsec after asserting MSYN. Cleared by Init or Clear Interface (bit 3) set to a logic '1'. Sets Error. READ ONLY.
13	Word Count Zero (WCZRO)	Set to indicate that the Word Count Register has incremented to zero. Sets Ready (bit 7) and causes Interrupt 0 or 1 if Interrupt Enable (bit 6) is set. READ ONLY.
12	Register Status	Set to indicate that PCMBA1 is in use. A zero indicates that PCMBA0 is in use. Cleared by Init or Clear Interface (bit 3) set to a logic '1'. Also cleared by Cycle set to a logic '0'. READ ONLY.
11	Frame Lock	Set to indicate the DECOM section is in frame lock. READ ONLY.
10	Subframe Lock	Set to indicate the DECOM section is in subframe lock. READ ONLY.
9	Start Subframe	Set to indicate that data transfer starts at the beginning of the subframe. A zero indicates that data transfer starts at the beginning of the frame. Cleared by Init or Clear Interface (bit 3) set to a logic '1'. READ/WRITE.
8	Search Data Xfer (SFXR)	Set to indicate that data will transfer in frame search, check or lock. A zero indicates that data will transfer only frame check or lock. READ/WRITE.
7	Ready	Set to indicate that the PCM interface is able to accept new commands. Set by Init, Clear Interface (bit 3) set to a one, Error, or Word Count Zero. Cleared by Go. READ ONLY.
6	Interrupt Enable	Set to allow Error or Word Count Zero to cause an interrupt. A Word Count Zero with PCMBA0 causes Interrupt 0. Likewise, Word Count Zero with PCMBA1 causes Interrupt 1. Cleared by Init or Clear Interface (bit 3) set to a logic '1'. READ/WRITE.
5	Extended Bus Address (XBA17) (XBA17)	Extended bus address bit 17, in conjunction with PCMBA0 and PCMBA1, specifies A(17:01) in DMA transfers. Cleared by Init or Clear Interface (bit 3) set to a logic '1'. XBA17 does not increment when PCMBA0 or PCMBA1 overflows; instead Error is set. READ/WRITE.
4	Extended Bus Address(XBA16)	Same as bit 5 above, except bus address bit 16. READ/WRITE.
3	Clear Interface	ORed with Init. Set to clear interface as does Init. WRITE ONLY.
2	Cycle	Set to enable the use of both PCMBA0 and PCMBA1 registers. When one register has finished its cycle, the other register will start. A zero will enable PCMBA0 and Interrupt 0 only. READ WRITE.
1	Not Used	
0	Go	Set to start the DMA process. Clears Ready. WRITE ONLY.

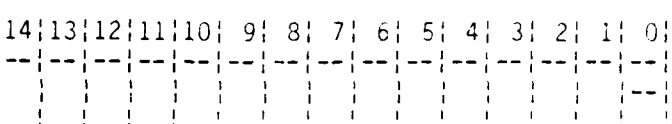
FIGURE 13 - DEVICE REGISTERS/DMA SECTION (COMMAND STATUS)

Data Buffer Register (PCMDBR) 764002 octal



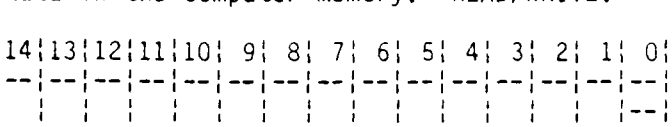
The Data Buffer Register is used for trouble shooting only. READ ONLY.

Buffer Address Register 0 (PCMBA0) 764004 octal



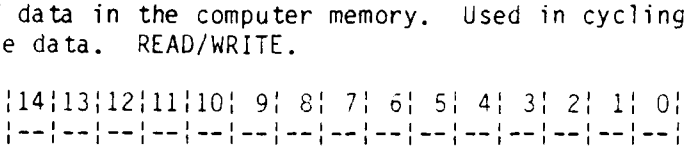
Buffer Address Register 0 controls the placement of data in the computer memory. READ/WRITE.

Buffer Address Register 1 (PCMBA1) 764006 octal



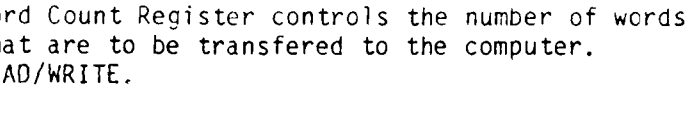
Buffer Address Register 1 controls the placement of data in the computer memory. Used in cycling the data. READ/WRITE.

Word Count Register (PCMWC) 764010 octal

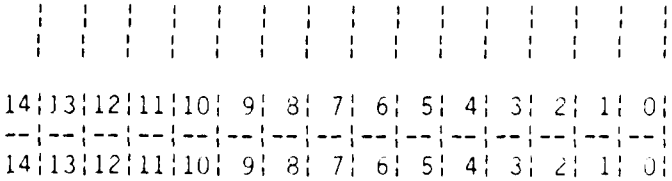


Word Count Register controls the number of words that are to be transfered to the computer. READ/WRITE.

Not Used 764012 octal

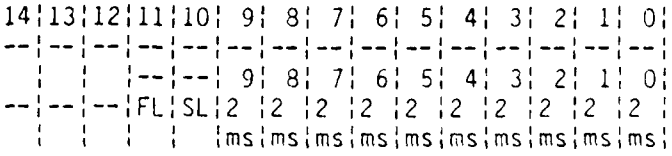


Time Data Register 0 (PCMTD0) 764014 octal



Time Data Register 0 contains timing information. READ ONLY.

Time Data Register 1 (PCMTD1) 764016 octal



Time Data Register 1 contains timing information and DECOM lock status. READ ONLY.

Interrupt Vector Address 0 = 170 octal
Interrupt Vector Address 1 = 174 octal
Prioity Level = BR5
Data Transfer = NPR

FIGURE 14 - DEVICE REGISTERS/DMA SECTION

C. System Specifications and Capabilities

1. Up to 2.0 megabits/sec.
2. Up to 16 bits/word.
3. Up to 1024 words/frame.
4. Up to 256 frames/subframe.
5. Up to 100 kiloword transfer rate to disk.
6. Up to 35 kiloword transfer rate to digital tape at 1600BPI.
7. Graphics display on the VT125 terminal.
8. Additional CRT displays, non graphic, on the two (2) auxiliary VT100 terminals.
9. High speed printout of text and graphics on the P300 line printer/ plotter.
10. A 300/1200 baud modem for transferring of data or programs to other computer systems.

D. Software

Two conflicting philosophies exist pertaining to software systems for this type of application. One school favors the "do all things for all people" approach, the other favors the small scale specialized approach. PSL chose the second approach. We will attempt to outline our approach and the reasons for this approach.

Operating Systems:

Two DEC furnished operating systems were considered for use on the PDP-11. RSX-11 is a rather large multi-tasking operating system designed primarily for the multi-user environment. RT-11 is a smaller, faster operating system designed primarily for the single user. For the usage envisioned, monitor and/or control of a single payload, RT-11 offered the best solution. Access to the I/O page, which is required in order to program the HS11-A DECOM/DMA interface, is straight forward under the RT-11 system. The approach under RSX-11 would have required writing a special purpose device driver and setting up a memory partition to allow communication between the DECOM/DMA task and the

application tasks. RT-11 with the XM monitor also offers a multi-processing capability.

SET UP Software:

An interactive program was written and provided to enable the user to program the DECOM/DMA interface and the bit sync. This program will either set up the system from an existing parameter file or prompt the user for all required information (see Figure 15). This allows the user to program the system one time for each different telemetry format to be supported and recall the parameters at a later time. Regardless of which path the user takes, all setup parameters are echoed to the CRT terminal for user verification before transmission to the DECOM/DMA interface and bit sync (see Figure 16). The DECOM section of the HS11-A and the bit sync are set up independently from the DMA section. This allows the DECOM and bit sync to be active and lock up to the PCM serial data with no DMA transfers.

Application Software:

After investigating the level of effort required to develop and maintain a general purpose display and data collection system it was determined that this would not be a cost effective solution. Due to the wide variety of sensors, data rates and project requirements, it was decided that special purpose "throw away" software packages would be the most timely and cost effective solution. The application software is written in FORTRAN IV and MACRO-11 (DEC's assembly language). The initial system was developed for support of an AFGL sounding rocket payload. This system required the display of sixty two (62) parameters. These parameters were divided into three (3) pages and displayed on two (2) CRT terminals in engineering units and as character string messages, as shown in Figure 17.

```
DO YOU WANT TO USE EXISTING SETUP INFO ? NO
DO YOU WANT TO SAVE SETUP INFO ? YES
ENTER FILE NAME OF NEW SETUP INFO (i.e. ??????.DAT) *ELKI.DAT
BITS PER WORD (MAX. = 16) ? 14
WORDS PER FRAME (MINOR) (MAX. = 1024) ? 44
FRAMES (MINOR) PER SUBFRAME (MAJOR) (MAX. = 256) ? 88
MSB FIRST ? YES
ACC ? NO
SUBFRAME SYNC LOCATION (0 = FIRST WORD PAST SYNC) ? 0
HOW MANY WORDS OF SYNC (MINOR) ? 1
HOW MANY WORDS OF SUBFRAME SYNC (MAJOR) ? 1

ENTER SYNC (MINOR)          MSB**************
PATTERN IN BINARY             11100110100000
ENTER SYNC (MINOR) MASK
PATTERN IN BINARY             11111111111111
ENTER SUBFRAME SYNC (MAJOR) **************
PATTERN IN BINARY             10110100000000
ENTER SUBFRAME SYNC (MAJOR)
MASK PATTERN IN BINARY        11111111111111
(MAX. = 64)
1 = COMPARE, 0 = NO COMPARE

Enter Bit Rate - 200.0 (in Kbit) : 1047.0
DETECTOR = I/R, Sample : SAMPLE
Loop Width = Narrow, Medium, Wide : WIDE
Source = 1, 2, 3 : 3
Polarity = Inverted, Normal : NORMAL
Input Code = NRZ-L, NRZ-M, NRZ-S
             DM/RZ, BIO-L, BIO-M, BIO-S : S



DO YOU WANT TO USE EXISTING SETUP INFO ? YES
ENTER FILE NAME OF EXISTING SETUP INFO  *ELKI.DAT
```

FIGURE 15- SET UP MENU

```
Bits per word = 14      Words per frame =    44      Frames per subframe =  88
MSB First
                                MSB**************
Frame (minor) Sync Pattern    = 11100110100000
Subframe (major) Sync Pattern = 10110100000000
Bit Rate =   1047.000 Kbit
Detector = Sample
Loop Bandwidth = 3.0%
Source 3
Positive Polarity (Normal)
Input Code = NRZ-S


Is the above information correct ? YES
```

FIGURE 16- SET UP PARAMETERS

```
 9:10:26

 ****** PAGE 1 DATA ******   LINK 1

UPPER DOOR NOT UNLATCHING          LOWER DOOR NOT UNLATCHING

NO SEPERATION                      NO LOGIC RESET

STARMAPPER DOOR CLOSED             LAB JACK MOTOR LOWERED

SENSOR DRIVE AND BRAKE-OFF         MOTOR BATTERY VOLTAGE =  30.4V

SUPPORT BATTERY VOLTAGE =  29.9V   LINK1 BATTERY VOLTAGE =  27.7V

LINK2 BATTERY VOLTAGE =  28.6V     BEACON BATTERY VOLTAGE =  31.2V

WELDMENT PRESSURE  =   12.9PSI     UPPER DOOR POSITION =  120.2DEG

LOWER DOOR POSITION =  119.6DEG

XMITTER TEMP LINK1 =   62.2C       XMITTER TEMP LINK2 =   65.2C

SHAFT ENCODER =       17
```

FIGURE 17- TYPICAL DATA PRINTOUT

The system user has the option of displaying any of these three pages on either CRT terminal. This arrangement allows two users to monitor different sets of parameters on a non-interference basis. Screen update rate is approximately once per second. This rate appears to minimize screen flicker while still providing an adequate refresh rate. Since the delivery of the prototype system to AFGL, PSL has used this hardware configuration and software approach to provide support to several other customers including other sounding rockets and surface to air missiles. Experience has shown that once requirements are defined, a display/data collection software system can be designed, implemented and tested in approximately four (4) man weeks.

E. Portability

The need for portability required shipping containers that would protect the equipment and not hinder the setup. SHOCK-STOP and RACK-PACK cases from Thermodyne International, Ltd. were used on the system. The high density polyethylene SHOCK-STOP cases come with full foam cushioning. The foam is custom cut to fit the equipment. The SHOCK-STOP cases are used in shipping the CRT terminals, line printer, and documentation. The RACK-PACK instrumentation case has an inner 19" rack frame built in. This frame is shock mounted to the ABS plastic outer shell with eight (8) elastometric shock mounts. Both the front and back covers remove quickly exposing the equipment for easy access. The RACK-PACK cases also come with four (4) removable casters on each case. The computer, disks, time code reader/ translator, PCM simulator, bit sync and digital tape drives are housed in these RACK-PACK instrumentation cases. These Thermodyne cases can be air shipped, if necessary. The system can be setup, checked out and ready to operate in less than two (2) hours.

SUMMARY/CONCLUSION

AFGL tasked PSL to develop a portable PCM telemetry station. The station was designed and built based on a DEC PDP-11/34A computer and a PSL built DECOM/DMA interface. Various peripherals are included with the station to enhance its capabilities. The PCM station was designed for Aries type sounding rockets, however, the station can process any PCM source that operates within the system specifications. The system has been successfully used on a recent AFGL Sounding Rocket Mission.

Planned system developments include: 1) interface of an Astro-Graph model 850 graphic recorder, adding strip chart capability; 2) programmable PCM bit synchronizer, with a bit rate up to 2 Mbit NRZ and 1 Mbit biphase; and 3) interface of the HS11-A DECOM/DMA to other computer systems.

END

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